INTEGRATED CIRCUITS PROTECTED AGAINST REVERSE ENGINEERING AND METHOD FOR FABRICATING THE SAME USING AN APPARENT METAL CONTACT LINE TERMINATING ON FIELD OXIDE

by

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I. BACKGROUND OF THE INVENTION

1. Field of the Invention.

This invention relates to the field of the prevention of reverse engineering of integrated circuits and/or making such reverse engineering so difficult and time-consuming as to make reverse engineering of integrated circuits non-feasible.

More particularly, this invention relates to using, in order to prevent and/or discourage such reverse engineering, apparent metal contact lines terminating on field oxide.

2. Description of the Related Art.

The design and development of semiconductor integrated circuits require thorough understanding of complex structures and

processes and involve many man-hours of work requiring high skill, costing considerable sums of money.

In order to avoid these expenses, some developers stoop to the contentious practice of reverse engineering, disassembling existing devices manufactured by somebody else, and closely examining them to determine the physical structure of the integrated circuit, followed by copying the device. Thus, by obtaining a planar optical image of the circuits and by studying and copying them, typically required, product development efforts are circumvented.

Such practices harm the true developer of the product and impairs its competitiveness in the market-place, because the developer had to expend significant resources for the development, while the reverse engineer did not have to.

A number of approaches have been used in order to frustrate such reverse engineering attempts, particularly in the field of semiconductor integrated circuits.

For instance, U.S. Patent No. 5,866,933 to Baukus, et. al. teaches how transistors in a complementary metal oxide-

semiconductor (CMOS) circuit can be connected by implanted, hidden and buried lines between the transistors. This hiding is achieved by modifying the p+ and n+ source/drain masks. The implanted interconnections are further used to make a 3-input AND-circuit look substantially the same as a 3-input OR-circuit.

Furthermore, US Patents Nos. 5,783,846 to Baukus, et. al. and 5,930,663 to Baukus et. al. teach a further modification in the source/drain implant masks, so that the implanted connecting lines between transistors have a gap inserted, the length of which is approximately the length of the feature size of the CMOS technology being used. These gaps are called "channel blocks."

If the gap is "filled" with one kind of implant (depending on whether the implanted connecting line is p or n), the line conducts; if another kind of implant is used for the gap-filling, the line does not conduct. The reverse engineer must determine connectivity on the basis of resolving the "n" or "p" implant at the minimum feature size of the channel block. In addition, transistor sizes and metal connection routings are modified, in order to deprive the reverse engineer of using clues which can help him find inputs, outputs, gate lines and so on as keys to the circuit functionality.

Practicing the inventions taught in the above-mentioned patents to secure an integrated circuit causes the reverse engineer to perform steps that are not always needed. These steps include: decomposing the circuit layer by layer, careful processing of each layer (which usually must include an etching step) followed by imaging of the layer with exact registration to other layers.

When the reverse engineer is delayering the circuit, he can look also for metal lines running from drain contacts to a poly-gate contact. He does this by looking in the two lowest metal layers for dimples, indicating the presence of metal plugs beneath. Thus, the contact position can be determined, greatly simplifying the reverse engineer's task. Previous patents mentioned above do not address this problem.

Therefore, there still exists a need for an inexpensive, easy-to-implement defensive method which can help to provide the enhanced protection against the reverse engineering of semiconductor integrated circuits, in particular to make the reverse engineer's task of finding real contacts to source and drains very difficult. The present invention provides such a method.

II. SUMMARY OF THE INVENTION

Usual practice of reverse engineering is to try to determine a basic structure of an integrated circuit by identifying metal patterns in the higher level metal layers in the circuit. Metals on these layers route the electric signals between circuit blocks. Once a basic circuit function is determined, rather than look at each next transistor pair, the reverse engineer will utilize the similarity in the upper metal patterns and assume each circuit section showing that pattern is the same.

The main objective of this invention is to make a reverse engineer to examine every connection of every CMOS transistor pair in an integrated circuit. If the reverse engineer is forced to do such detailed examination, he would have to spend so much time and money as to make the attempt of reverse engineering prohibitive and leading to *de facto* protection against reverse engineering.

In order to achieve this objective, circuit techniques are used to make the pattern of a subsequent circuit section unpredictable and non-repeatable; in other words, these techniques make it incorrect to make a usual assumption that similar metal patterns encompass similar circuit functionality.

The gist of this invention is to guide the reverse engineer to an erroneous assumption by having some metal traces terminate on field oxide located close to a contact region. He will assume, erroneously, that the presence of the plug is to make a real contact to a source or drains when, in fact, there is none.

The field oxide that defines and borders on the contact area is offset so that it covers a portion of the contact area. Then, the dimple and the metal plug are aligned so that the metal plug ends on the field oxide adjacent to the source of drain.

The patterns will appear identical, but these apparent connections are not real connections. The reverse engineer will be led to the wrong conclusion as to the circuit block functionality as a result.

A first aspect of the invention provides a semiconducting device adapted to prevent and/or to thwart reverse engineering, comprising field oxide layer disposed on a semiconductor substrate, a metal plug contact disposed within a contact region and above said field oxide layer, and a metal connected to said metal plug contact.

A second aspect of the invention provides a method for preventing and/or thwarting reverse engineering, comprising steps of providing a field oxide layer disposed on a semiconductor substrate, providing a metal plug contact disposed within a contact region and above said field oxide layer, and connecting a metal to said metal plug contact.

A third aspect of the invention provides a semiconducting device adapted to prevent and/or to thwart reverse engineering, comprising field oxide layer disposed on a semiconductor substrate, a metal plug contact disposed outside a contact region and above said field oxide layer, and a metal connected to said metal plug contact.

A fourth aspect of the invention provides method for preventing and/or thwarting reverse engineering, comprising steps of providing a field oxide layer disposed on a semiconductor substrate, providing a metal plug contact disposed outside a contact region and above said field oxide layer and connecting a metal to said metal plug contact.

III. BRIEF DESCRIPTION OF THE DRAWINGS

The features and advantages of the present invention will become better understood with regard to the following description, appended claims, and accompanying drawings where

FIG. 1 schematically shows a prior art field effect transistor that could be part of a CMOS integrated circuit.

FIG. 1(a) schematically shows how a contact plug is usually located relative to field oxide in (also prior art).

FIG. 1(b) schematically shows relative locations of the metal plug and the metallization layer.

FIG. 2 is a schematic diagram showing a preferred embodiment of this invention.

FIG. 3 is a schematic diagram showing an alternative embodiment of this invention.

IV. DETAILED DESCRIPTION OF THE INVENTION

This invention can be used on any semiconducting device utilizing, preferably, CMOS integrated circuits or bipolar

silicon circuits.

FIG. 1 shows general architecture of some elements of a typical field effect transistor within a CMOS integrated circuit 100. The circuit 100 comprises a source 1, a drain 2, gate oxide 3, an insulating field oxide 4, preferably, silicon oxide. It further comprises a layer of polysilicon ("poly") 5, of silicide 6, and a contact plug 7. The circuit 100 is disposed on a semiconducting substrate 8.

FIG 1(a) demonstrates how a contact plug 7 is positioned relative to field oxide 4 in prior art. The contact plug 7 is disposed over a layer of silicide 6 and over the active area 9. In FIG. 1, such a contact could be placed over both the source 1 and the drain 2.

FIG. 1(b) shows that the contact plug 7 is disposed orthogonally to the plane of metallization layer 10. Such relative orientation of the contact plug 7 is present both in prior art and in this invention.

Seeing metallization 10, a reverse engineer will presume that it leads to either the source or the drain 2, or the gate. He will

be misled and confused when the metal leads to the field oxide 4, as shown on FIG. 2 as a preferred embodiment of this invention.

FIG. 2 shows a contact plug 7 and the contact is meant to be to the right of field oxide 4. Field oxide 4 is deposited over a portion of the contact region, and the metal plug 7 which would have usually been placed to end on the contact region ends up on the field oxide 4 region instead.

The plug 7 typically has a substantially smaller area than the contact region.

L_{10} is the overlap area between the oxide region, the normal contact region and the placing of the plug 7. The diameter of the plug 7 is preferably not larger than the size of the minimum feature. L_{10} can be of any size, specified by the fabrication vendor, and is preferably 10% larger than the size of the minimum feature. A preferred contact dimension is up to about three times of the via size.

Alternatively, the plug 7 could also end on an oxide layer 4 deposited somewhere in the circuit where there would not be a contact. FIG. 3 shows such embodiment. As can be seen from FIG.

3, contact plug 7 does not extend into active area 9. Instead it ends on oxide layer 4.

Having described the invention in connection with several embodiments thereof, modification will now suggest itself to those skilled in the art. As such, the invention is not to be limited to the described embodiments except as required by the appended claims.